UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,586	08/19/2003	Nicolas I. Kacevas	02207/684502	2935

23838 7590 10/31/2006

KENYON & KENYON LLP
1500 K STREET N.W.
SUITE 700
WASHINGTON, DC 20005

EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,586	KACEVAS, NICOLAS I.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-20 are rejected on the ground of nonstatutory double patenting over claim1-23 of U. S. Patent No. 6,643,770 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: The claims of the instant application and the patent are presented side by side below with explanations which show that the claims of the application are obvious in view of the claims of the patent.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Patent 6,643,770	Instant Application
	1. a bus;
1. A method for branch misprediction recovery in a multi-stage pipelined processor, the method comprising: predicting at a branch, an instruction sequence predicted to be executed and an instruction sequence predicted not to be executed; advancing an instruction in the instruction sequence that is predicted not to be executed through a plurality of instruction pipeline stages for execution; storing to a mispredicted path side memory, each stage in parallel, a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages;	an external memory coupled to the bus; a processor coupled to the memory via the bus, the processor to receive a plurality of instructions from the memory, wherein the processor is to:
advancing an instruction in the instruction sequence predicted to be executed through the plurality of instruction pipeline stages for execution after the instruction in the instruction sequence that is predicted not to be executed is advanced;	advance an instruction in an instruction sequence predicted not to be executed through an instruction pipeline, store in a mispredicted path memory in parallel to the instruction pipeline as a result of the instruction in the instruction sequence that is

Patent	Instant Application
determining if the instruction in the instruction sequence predicted to be executed was predicted correctly; and if the instruction in the instruction sequence predicted to be executed was mispredicted, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	predicted not to the be executed from the instruction pipeline; and restore in parallel the result from the mispredicted path side memory into the instruction pipeline for continued execution if an instruction in an instruction sequence predicted to be executed is mispredicted.
2. The method of claim 1, the method further comprises: if the instruction in the instruction sequence predicted to be executed was predicted correctly, discarding the stored result of the instruction that is predicted not to be executed.	3. The system of claim 2, wherein the processor is to further: discard the stored result of the instruction that is predicted not to be executed if the instruction in the sequence predicted to be executed is was predicted correctly.
3. The method of claim 1, the method further comprises: predicting that another instruction will be executed; advancing the another instruction through the plurality of stages; determining if the another instruction was predicted correctly; and if the another instruction was not predicted	2. the system of claim 2, wherein the processor is to further: advance the instruction in the instruction sequence predicted to be executed through the instruction pipeline.

Patent	Instant Application
correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	
3. The method of claim 1, the method further comprises: predicting that another instruction will be executed; advancing the another instruction through the plurality of stages; determining if the another instruction was predicted correctly; and if the another instruction was not predicted correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	4. the system of claim 2, wherein the processor is to further predict that another instruction will be executed; advance the another instruction through the instruction pipeline; determine if the another instruction was predicted correctly; and restore in parallel the result into the instruction pipeline for continued execution if the another instruction was predicted correctly.
4. The method of claim 1, wherein the restoring operation comprises restoring the result from the mispredicted branch side memory.	

Patent	Instant application
5. The method of claim 1, wherein the mispredicted branch side memory comprises a First-In, First-Out memory.	
6. The method of claim 1, wherein the mispredicted branch side memory comprises a cache memory.	5. wherein the mispredicted path side memory is a cache located internal to the processor.
7. The method of claim 1, wherein the storing operation and restoring operation are performed with respect to the same pipeline stage.	
8. The method of claim 1, wherein a plurality of instruction pipeline stages are a defined optimal number of stages.	
1. A method for branch misprediction recovery in a multi-stage pipelined processor, the method comprising: predicting at a branch, an instruction sequence predicted to be executed and an instruction sequence predicted not to be executed;	7. the method of claim 6, further comprises predicting at a branch the instruction sequence predicted to be executed and the instruction sequence not to be executed.

Patent

advancing an instruction in the instruction sequence that is predicted not to be executed through a plurality of instruction pipeline stages
for execution; storing to a mispredicted path side memory, each stage in parallel, a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages; advancing an instruction in the instruction sequence predicted to be executed through the plurality of instruction pipeline stages for execution after the instruction in the instruction sequence that is predicted not to be executed is
advanced; determining if the instruction in the instruction sequence predicted
to be executed was predicted correctly; and if the instruction in the instruction sequence predicted to be executed was mispredicted, restoring in parallel the result from the storing operation into the plurality of
instruction pipeline stages for continued execution.

Instant application

6. A method for branch misprediction recovery in a multi-stage pipelined processor, the method comprising:

advancing an instruction in an instruction sequence predicted not to be executed through a plurality of pipeline stages

storing in a mispredicted path side memory, each stage in parallel, a result of the instruction sequence that is predicted not to be executed from a plurality of instruction pipeline stages; and

Restoring in parallel the operation into a plurality of instruction pipeline stages for continued execution if an instruction in an instruction sequence predicted to be executed is mispredicted.

Patent	Instant application
2. The method of claim 1, the method further comprises: if the instruction in the instruction sequence predicted to be executed was predicted correctly, discarding the stored result of the instruction that is predicted not to be executed.	8. The method of claim 6, the method further comprises: if the instruction in the instruction sequence predicted to be executed was predicted correctly, discarding the stored result of the instruction that is predicted not to be executed.
3. The method of claim 1, the method further comprises: predicting that another instruction will be executed; advancing the another instruction through the plurality of stages; determining if the another instruction was predicted correctly; and if the another instruction was not predicted correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	9. The method of claim 6, the method further comprises: predicting that another instruction will be executed; advancing the another instruction through the plurality of stages; determining if the another instruction was predicted correctly; and if the another instruction was not predicted correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.

Patent	Instant Application
15. Apparatus for branch misprediction recovery, comprising: a branch prediction unit to predict, at a branch, that an instruction sequence will be executed and an instruction sequence will not to be executed; a plurality of instruction pipeline stages to advance an instruction in the instruction sequence that is predicted not to be executed and to advance an instruction in the instruction sequence predicted to be executed through the plurality of instruction pipeline stages for execution after the instruction in the instruction sequence that is predicted not to be executed is advanced; a mispredicted path side memory, coupled to the plurality of instruction pipeline stages, to store in parallel a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages; a branch execution unit to determine if the instruction in the instruction sequence predicted to be executed was predicted correctly and if the instruction in the instruction sequence predicted to be executed was	11. the apparatus of claim 10 further comprising a a branch prediction unit to predict, at a branch, that an instruction sequence will be executed and an instruction sequence will not to be executed. 10. Apparatus for branch misprediction recovery comprising: a plurality of instruction pipeline stages to advance an instruction in the instruction sequence that is predicted not to be executed mispredicted path side memory, to store in parallel to the instruction pipeline stages a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages;and a branch execution unit to determine if the instruction in the instruction sequence predicted to be executed is predicted mispredicted and if the instruction in the instruction sequence predicted to be executed is

Patent

mispredicted, the branch execution unit restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.

16. The apparatus of claim 15, wherein the branch execution unit comprises: a non-predicted memory control unit to transmit a read mispredicted path side memory signal to the non predicted path side memory and in response, the non-predicted path side memory is to restore the result into the plurality of instruction pipeline stages in parallel.

17. The apparatus of claim 15, further comprises: a non-predicted data line that is to couple each stage of the plurality of instruction pipeline stages to
the mispredicted path side memory and to transfer a result from that stage to the mispredicted path side memory.

Instant Application

mispredicted, the branch execution unit to restore in parallel the result from the mispredicted path side memory into the plurality of instruction pipeline stages for continued execution.

12. The apparatus of claim 10, further comprising: a mispredicted memory control unit to transmit a read mispredicted path side memory signal to the mis predicted path side memory and in response, the mispredicted path side memory is to restore the result into the plurality of instruction pipeline stages in parallel.

13. The apparatus of claim 10, further comprises: a mispredicted data line that is to couple each stage of the plurality of instruction pipeline stages to
the mispredicted path side memory and to transfer a result from that stage to the mispredicted path side memory.

Patent	Instant Application
18. The apparatus of claim 17, further comprises: a recovery path data line that is to couple each stage of the plurality of instruction pipeline stages to the mispredicted path side memory and to restore a result from the mispredicted path side memory to that stage.	14. The apparatus of claim 13, further comprises: a recovery path data line that is to couple each stage of the plurality of instruction pipeline stages to the mispredicted path side memory and to restore a result from that stage to the mispredicted path side memory.
17. The apparatus of claim 15, further comprises: a non-predicted data line that is to couple each stage of the plurality of instruction pipeline stages to the mispredicted path side memory and to transfer a result from that stage to the mispredicted path side memory.	
19. The apparatus of claim 18, further comprises: a multiplexer that is coupled at a first input to a stage of the plurality of pipeline stages via an input data line and is coupled at a second input to the mispredicted path side memory via the recovery path data line.	15. The apparatus of claim 13, further comprises: a multiplexer that is coupled at a first input to a stage of the plurality of pipeline stages via an input data line and is coupled at a second input to the mispredicted path side memory via the recovery path data line.

Patent	Instant Application
20. The apparatus of claim 19, wherein the multiplexer is coupled at an output to a next stage via an output data line and is coupled at the output to the mispredicted path side memory via the mispredicted data line.	16. The apparatus of claim 15, wherein the multiplexer is coupled at an output to a next stage via an output data line and is coupled at the output to the mispredicted path side memory via the mispredicted data line.
15. Apparatus for branch misprediction recovery, comprising: a branch prediction unit	17. Apparatus for branch misprediction recovery,the system comprising: a bus an external memory coupled to the bus a processor coupled to the memory via the bus , the processor to receive a plurality of instructions from the memory wherein the processor is to: predict at a branch, an instruction sequence predicted to be executed and an instruction sequence predicted not to be executed; advance an instruction in the instruction sequence that is predicted not to be executed through a plurality of instruction pipeline stages for execution; store to a mispredicted path side memory, each stage in parallel to the plurality of instruction pipeline stages a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of pipeline stages; advance an instruction in the instruction sequence predicted not to be executed
to predict, at a branch, that an instruction sequence will be executed and an instruction sequence will not to be executed; a plurality of instruction pipeline stages to advance an instruction in the instruction sequence that is predicted not to be executed and to advance an instruction in the instruction sequence predicted to be executed through the plurality of instruction pipeline stages for execution after the instruction in the instruction sequence that is predicted not to be executed is advanced; a mispredicted path side memory, coupled to the	

Patent	Instant application
plurality of instruction pipeline stages, to store in parallel a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages; a branch execution unit to determine if the instruction in the instruction sequence predicted to be executed was predicted correctly and if the instruction in the instruction sequence predicted to be executed was mispredicted, the branch execution unit restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	Executed through a plurality of instruction pipeline stages for execution after the instruction in the instruction sequence that is predicted not to be executed is advanced; Determine if the instruction sequence predicted to be executed was predicted correctly Restore in parallel the resultfrom the storing operation into a plurality of instruction pipeline stages for continued execution if the instruction in the instruction sequence predicted to be executed was mispredicted.
2.The method of claim 1, the method further comprises: if the instruction in the instruction sequence predicted to be executed was predicted correctly, discarding the stored result of the instruction that is predicted not to be executed.	18. The method of claim 17, wherein the processor is to further discard the stored result of the instruction that is predicted not to be predicted correctly.

Patent	Instant application
3. The method of claim 1, the method further comprises: predicting that another instruction will be executed; advancing the another instruction through the plurality of stages; determining if the another instruction was predicted correctly; and if the another instruction was not predicted correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.	19. The system of claim 17, wherein the processor is to further: predict that another instruction will be executed; advance the another instruction through the instruction pipeline stages; determine if another instruction was predicted correctly; and restore in parallel the result from the store into the plurality of instruction pipeline stages for continued execution if the another instruction was not predicted correctly.
22. The apparatus of claim 15, wherein the mispredicted path side memory comprises a cache memory.	20. The system of claim 17, wherein the mispredicted path side memory is a cache memory located internal to the processor.

As can be seen above the claims of the instant application are substantially the same as the claims of the patent. The ordering and placement of various features have been changed in the claims of the application. Also features which are well known in the art and would have been obvious to one of ordinary skill are part of the claims of the application that were not included in the claims of the patent. Namely an external memory and bus coupled to the memory and the processor coupled to the memory via the external bus. The hierarchical memory for storing data and/or instruction such as in a slower larger memory was well known in the art at the time of the claimed invention at least to provide for storage and access to data and instructions that were not currently being used in a executing program.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of meaning of claim 2 is unclear because claim 2 depends upon itself. Likewise since claims 3-5 depend from claim 2 they contain that same ambiguity as to scope contained in claim 2.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jourdan etal. (IEEE article entitled The effects of mispredicted-path execution of branch prediction structures) disclosed the effects of mispredicted path execution on branch prediction structures (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC